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(54) NANOFABRICATION OF NANOPOROUS (52) U.S. Cl.
ARRAYS CPC

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(57) **ABSTRACT**

An array having nanopores is produced by coating a thin layer

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on the metal or other material by combining a first polymer

on the metal or other material by c (22) Filed: **Jun. 30, 2015** on the metal or other material by combining a first polymer (22) Filed: **Jun. 30, 2015** Related U.S. Application Data nanodomains of the first polymer in the second polymer
resulting in the formation of a uniform hexagonal pattern of (60) Provisional application No. 62/020,259, filed on Jul. 2, the first polymer nanodomains in the second polymer over entire surface of the metal or other material. The nan Publication Classification odomains are removed by etching to form nano-voids that extend through the polymer layer. Nanopores are created in (51) Int. Cl. the metal or other material layer by ion beam milling the metal or other material layer by ion beam milling the BOLD 67.1 (1) metal through the nano-voids to produce nano-pores that
BOLD extend through the metal or other material creating an array (1) extend through the metal or other material creating an array
having nanopores. having nanopores.

FIG.1

FIG. 11A

FIG.11B

NANOFABRICATION OF NANOPOROUS ARRAYS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to and benefit under 35 U.S.C. S 119(e) of U.S. Provisional Patent Application No. 62/020.259 filed Jul. 2, 2014 entitled "High Fidelity Macros cale Coverage of Nanoporous Metal Arrays Via Lift-Off-Free Nanofabriaction," the content of which is hereby incorporated by reference in its entirety for all purposes.

STATEMENT AS TO RIGHTS TO APPLICATIONS MADE UNDER FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

[0002] The United States Government has rights in this application pursuant to Contract No. DE-AC52-07NA27344 between the United States Department of Energy and Lawrence Livermore National Security, LLC for the opera tion of Lawrence Livermore National Laboratory.

BACKGROUND

[0003] 1. Field of Endeavor

[0004] The present application relates to nanolithography and more particularly to nanolithography for creating nan oporous arrays.

[0005] 2. State of Technology
[0006] This section provide

This section provides background information related to the present disclosure which is not necessarily prior art.

0007 United States Published Patent Application No. 2013/0245416 for a nanoporous metal multiple electrode array and method of making same provides the following state of technology information. A method is disclosed for fabricating a low-impedance nanoporous metal multiple elec trode array for measuring electrophysiology activity. A pat terned photoresist is applied to a substrate, in which the patterned photoresist corresponds to a pattern of the nanopo rous metal multiple electrode array. A metal alloy including a sacrificial alloying element is deposited in the pattern of the nanoporous metal electrode array. The patterned photoresist is removed to expose the metal alloy as deposited. At least part of the sacrificial alloying element is removed from the metal alloy to create nanoporous metal electrode tips thereby forming the nanoporous metal multiple electrode array. The resultant nanoporous metal multiple electrode array has improved impedance characteristics in comparison to con ventional multiple electrode arrays.

[0008] U.S. Pat. No. 8,512,588 for a method of fabricating a scalable nanoporous membrane filter provides the following state of technology information. A method of fabricating a nanoporous membrane filter having a uniform array of nan opores etch-formed in a thin film structure (e.g. (100)-ori ented single crystal silicon) having a predetermined thick ness, by (a) using interferometric lithography to create an etch pattern comprising a plurality array of unit patterns having a predetermined width/diameter, (b) using the etch pattern to etch frustum-shaped cavities or pits in the thin film structure such that the dimension of the frustum floors of the cavities are substantially equal to a desired pore size based on the predetermined thickness of the thin film structure and the predetermined width/diameter of the unit patterns, and (c) removing the frustum floors at a boundary plane of the thin film structure to expose, open, and thereby create the nanop ores substantially having the desired pore size.

[0009] United States Published Patent Application No. 2005/0255581 for self-organized nanopore arrays with con trolled symmetry and order provides the following state of technology information. An ordered, single domain nanopore array having a macroscale area in a first material is provided. A method of making a nanopore arrays with a controlled pattern include providing a substrate comprising a first surface having a first pattern, depositing a first material capable of forming nanopores onto said first-Surface having the first pattern, and anodically oxidizing said first material to form the nanopore array with the controlled pattern in the anodi cally oxidized first material.

[0010] U.S. Pat. No. 8,786,852 for nanoscale array structures suitable for surface enhanced Raman scattering and methods related thereto provides the following state of tech nology information. Methods for fabricating nanoscale array structures suitable for Surface enhanced Raman scattering, structures thus obtained, and methods to characterize the nanoscale array structures suitable for surface enhanced Raman scattering. Nanoscale array structures may comprise nanotrees, nanorecesses and tapered nanopillars.

SUMMARY

[0011] Features and advantages of the disclosed apparatus, systems, and methods will become apparent from the follow ing description. Applicant is providing this description, which includes drawings and examples of specific embodi ments, to give a broad representation of the apparatus, sys tems, and methods. Various changes and modifications within the spirit and scope of the application will become apparent to those skilled in the art from this description and by practice of the apparatus, systems, and methods. The scope of the apparatus, systems, and methods is not intended to be limited to the particular forms disclosed and the application covers all modifications, equivalents, and alternatives falling within the spirit and scope of the apparatus, systems, and methods as defined by the claims.

[0012] Posing superior properties, nanoporous metals have been drawing attractions in a wide range of applications. For example, they possess a much higher surface area suitable for better electron transfer which can lead to an improved per formance of an electrode in an electric double layer capacitor or a battery or a photovoltaic cell. They offer an increased number of available sites for the adsorption of analytes, typi cally a highly desirable feature for sensors. At certain wave lengths, they can facilitate an anomalous enhancement of the transmitted light through the tunneling of surface plasmons, a feature widely exploitable by light emitting devices, plas monic lithography, refractive-index-based sensing, and all optical Switching. Furthermore, low molecular detection lim its can be obtained by Surface enhanced Raman spectroscopy (SERS) via intense electromagnetic field concentration at hot spots that these nanoporous metals provide.

[0013] The inventor's apparatus, systems, and methods provide the production of an array having nanopores. A substrate of silicon or other materials is provided. The substrate has a flat surface. A thin layer of metal or other material is applied to the flat surface of the substrate in a manner that provides a uniform flat surface on the metal or other material. A mask is created on the uniform flat surface of the metal or other material by combining a first polymer and a second polymer to form a polymer layer of the first and second polymer. The first polymer self-assembles into nanodomains of the first polymer in the second polymer. The self-assembly of the nanodomains results in the formation of a uniform hexagonal pattern of the first polymer nanodomains in the second polymer over the entire uniform flat surface on the metal or other material. The nanodomains are removed by etching to form nano-voids that extend through the polymer layer. Nanopores are created in the metal or other material by ion beam milling the metal through the nano-voids to produce nano-pores that extend through the metal or other material creating the array having nanopores.

[0014] The inventor's array having nanopores has use in batteries, ultracapacitors, other electrical devices, and any device that utilizes an array with nanopores. The inventor's array having nanopores possess a much higher surface area suitable for better electron transfer providing improved per formance of an electrode in an electric double layer capacitor or a battery or a photovoltaic cell.

[0015] The apparatus, systems, and methods are susceptible to modifications and alternative forms. Specific embodi ments are shown by way of example. It is to be understood that the apparatus, systems, and methods are not limited to the particular forms disclosed. The apparatus, systems, and meth ods coverall modifications, equivalents, and alternatives fall ing within the spirit and scope of the application as defined by the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are incorporated into and constitute a part of the specification, illustrate specific embodiments of the apparatus, systems, and methods and, together with the general description given above, and the detailed description of the specific embodiments, serve to explain the principles of the apparatus, systems, and methods.

0017 FIG. 1 is a flow chart that illustrates the inventor's nanolithography method for creating an array on a film of metal or other material.

[0018] FIG. 2 illustrates additional details of the step of providing a substrate.

[0019] FIG. 3 illustrates additional details of the step of coating metal or other material on the surface of the substrate.

[0020] FIGS. 4A and 4B illustrate additional details of the step of coating a polymer layer on the surface of the metal or other material described in greater detail.

[0021] FIGS. 5A and 5B illustrate the coating of a polymer layer on the metal or other material layer by combining a first polymer and a second polymer that form self-assembled nan odomains of the first polymer in the second polymer.

[0022] FIGS. 6A and 6B illustrate removal of the nanodomains by etching leaving nanovoids in the polymer layer. [0023] FIG. 7 illustrates ion beam milling the metal or other material layer through the nanovoids in the polymer layer mask.

0024 FIGS. 8A and 8B illustrate removal of the polymer layer mask leaving the nanoporous array.

0025 FIG.9 is an illustration of the inventor's nanolithog raphy method for producing a nanoporous array.

[0026] FIG. 10 illustrates a nanolithography method for producing a nanoporous array battery.

0027 FIGS. 11A and 11B illustrate nanolithography methods for producing nanoporous filters.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0028] Referring to the drawings, to the following detailed description, and to incorporated materials, detailed information about the apparatus, systems, and methods is provided including the description of specific embodiments. The detailed description serves to explain the principles of the apparatus, systems, and methods. The apparatus, systems, and methods are susceptible to modifications and alternative forms. The application is not limited to the particular forms disclosed. The application covers all modifications, equiva lents, and alternatives falling within the spirit and scope of the apparatus, systems, and methods as defined by the claims.

[0029] There exist various methods of creating random nanoporous metal over a large area Such as de-alloying, elec trochemical deposition, and organic patterning. An ordered array of nanopores, on the other hand, could be directly pat lithography if a tiny area is sufficient. Coverage of a large metal area with an array of nanopores, however, requires a lengthy procedure generally including lithography followed by lift-off. The lift-off process can be a real challenge, par ticularly when the density of the array is very high. Retention or total peel-off can, for example, occur when the side walls of a sacrificial nanospacer are excessively coated. Reproducibil ity and uniformity of lift-off canthus be problematic when the pitch size goes below 40-50 nm. Therefore, a lift-off-free technique has been desired in order to produce a highly dense, nanoporous metal array.

[0030] Realizing uniform and wafer-scale coverage of ultradense arrays of nanopores on metal thin films is still a big challenge with the current nanomanufacturing methods. The inventors in one or more of their research projects have estab lished a low-cost, high-throughput, lift-off-free nanolitho graphic method for creating hexagonal arrays of sub-30-nmsized pores on a metal film, achieving uniform coverage over an entire wafer of 10 cm in diameter. Spherical nanodomains of poly(methyl methacrylate) (PMMA) were demonstrated to be well-controlled and self-aligned within a polystyrene (PS) matrix layer on a metal thin film without any intermediary coating. After removal of PMMA, the porous PS thin film acts as an etch mask for defining nanoscale pores in the metal underlayer by argon ion beam milling, resulting in wafer scale patterning with great fidelity. Conditions for such uniformity control of the nanopore arrays critically depend on the initial roughness of the metal layer, from which the best parametric conditions are deduced.

[0031] Referring now to the drawings and in particular to FIG. 1, a flow chart illustrates the inventor's nanolithography method for creating an array on a film of metal or other material. The flowchart is designated generally by the refer ence numeral 100. The inventor's nanolithography method for creating an array on a film of metal or other material provides the production of an array having nanopores.

 $[0032]$ As illustrated in FIG. 1, the nanolithography method for creating an array 100 includes the steps described below [0033] Step 1—Providing a substrate having surface. A substrate of silicon or other materials is provided. The sub strate has a flat surface. The step 1 of providing a substrate having surface is designated by the reference numeral 101.

[0034] Step 2—Coating metal or other material on the surface of the substrate. A thin layer of metal or other material is applied to the flat surface of the substrate in a manner that provides a uniform flat surface on the metal or other material. This provides an exposed surface of the metal or other mate rial for additional processing. The step 2 coating of metal or other material on the surface of the substrate is designated by the reference numeral 102.

0035) Step 3—Forming a mask on the exposed metal or other material Surface by combining a first polymer and a second polymer to form self-assembled nanodomains of the first polymer in the second polymer and removing the nan odomains to form nano-Voids in the mask. A mask is created combining a first polymer and a second polymer to form a polymer layer of the first and second polymer. The first poly merself-assembles into nanodomains of the first polymer in the second polymer. The self-assembly of the nanodomains results in the formation of a uniform hexagonal pattern of the first polymer nanodomains in the second polymer over the entire uniform flat surface on the metal or other material. The nanodomains are removed by etching to form nano-Voids that extend through the polymer layer. The step 3 of forming a mask is designated by the reference numeral 103.

[0036] Step 4—Ion beam milling the metal or other material through the nano-voids of the mask producing nano-pores in the metal or other material creating the array. Nanopores are created in the metal or other material by ion beam milling the metal through the nano-voids to produce nano-pores that extend through the metal or other material creating the array having nanopores. The step 4 of ion beam milling is designated by the reference numeral 104.

[0037] Referring now to FIG. 2 the step of providing a substrate is illustrated in greater detail. The overall illustra tion of providing a Substrate is designated generally by the reference numeral 200. A substrate 202 of silicon or other material is provided. The substrate 202 has a flat surface 204. [0038] In one embodiment the inventors used a 10 centimeter diameter silicon waferas the substrate 202; however it is to be understood that other size silicon wafers and substrates of other materials can be used as the substrate 202. For example, substrates of silicon dioxide, aluminum oxide, sapphire, germanium, gallium arsenide, polyethylene terephthalate, polyethylene-naphthalate, polyimide, paper, foil can be used as the substrate 202. Substrates are chosen for the end use envi ronment of the finished array. For example if a flexible array is to be produced the material for the substrate is chosen to be flexible.

[0039] Referring now to FIG. 3 the step of coating metal or other material on the surface of the substrate is illustrated in greater detail. A thin layer 300 of metal or other material is applied to the flat surface 204 of the substrate 202 in a manner that provides a uniform planar surface 302 on the metal or other material. This provides an exposed surface 302 of the metal or other material for additional processing.

[0040] The surface 302 of the metal or other material 300 is smooth. In determining the best roughness of surface 302 the inventors deposited Au on bare Si wafers with various thicknesses from 30 nm to 200 nm in order to obtain various surface roughness values. In a first sample, 30-nm-thick Au was deposited on a 30-nm-thick Pt layer. In additional samples, thicknesses of Au deposited directly on Si were 30, 50, 100, 150 and 200 nm, respectively. Au deposition rate for the first sample was faster than for the other samples. The roughness of the Authin film generally increases with the film thickness. The additional process still takes place even for a rather rough surface (Rrms $>$ 20 Å), but it is actually the pore coverage that is strongly influenced by the metal film rough ness. The first sample was the smoothest sample (Rrms of 6.5 Å), the pore coverage was 91.9 (\pm 1.1)%. Surprisingly, a slight variation in Rrms can give rise to considerable degradation in the pore coverage. With increased roughness, uniformity also decreases. Although the inventors had to deposit a thin film to control the surface roughness, they envisioned that it is possible to obtain large pore coverage even for thicker metal films by lowering the Surface roughness via optimization of deposition parameters. Strategies to improve the smoothness of as-deposited metal films encompass changing metal depo sition rate adjusting the temperature of a destination substrate coating a sticking agent layer prior to deposition, and per forming a template-striping method.

[0041] In an attempt to assess the quality of the inventors nanoporous metal films, they defined a term, pore coverage, mentally and theoretically extrapolated for ideal conditions. This pore coverage measures 91.9% for the inventor's nan oporous metal films over a 10-cm-diameter wafer with a great uniformity value of 99%. The inventors characterize that the pore coverage becomes lower as the metal film gets rougher. In order to explain the relationship between pore coverage and roughness, the inventors introduced the effect of rough localities of the metal surface on BCP self-assembly by ana lyzing how they could impede the mobility of PS molecules thereby creating defect sites on the nanoporous PS and even tually on the nanoporous metal arrays. Finally, the inventors propose a method to estimate an expected pore coverage value for any given metal roughness by taking into account the areal density of the rough localities.

[0042] Referring now to FIGS. 4A and 4B the step of coating a polymer layer on the surface of the metal or other material is illustrated in greater detail. As shown in FIG. 4A, a polymer layer 400 is coated on the surface of the metal or other material 300. The polymer layer 400 will be used to create a mask for further processing.

[0043] FIG. 4B is a greatly enlarged cut away section of the polymer layer 440, metal or other material layer 300 and substrate 202. The greatly enlarged cut away section will be used in FIGS. 5, 6, 7, and 8 and in the following description of the polymer layer 400 being used to create a mask.

0044) Referring now to FIGS. 5A and 5B the forming a mask on the exposed metal or other material Surface by com bining a first polymer and a second polymer that form self assembled nanodomains of the first polymer in the second polymer is illustrated in greater detail. As illustrated in FIG. 5A, the polymer layer 400 has been coated on the metal or other material layer 300. The polymer layer 400 is made of a first polymer 500a and a second polymer 500b.

[0045] By selecting the composition of the first polymer 500a and the second polymer 500b and by controlling the application of the polymer layer 400 the inventors have dis covered that it is possible to pattern nanodomains of polymer 500a in polymer 500b. The nanodomains are formed directly on the material 300 at macroscales without use of any inter mediary. Suitable nanodomains can be formed by lowering
the roughness of the destination material 300 and controlling the application of the polymer layer 400 to pattern nanodomains of polymer $500a$ in polymer $500b$. The nanodomains can be in the form of cylindrical, spherical, lamellar blocks, or other shapes of different polymerized monomers. Compared with spherical nanodomains, cylindrical nan odomains have been more useful due to their high aspect ratio and negligible residual layers.

[0046] The application of the polymer layer 400 results in the first polymer 500a self-assembling into nanodomains of the first polymer $500a$ in the second polymer $500b$. The self-assembly of the nanodomains results in the formation of a uniform hexagonal pattern of the first polymer nan odomains $500a$ in the second polymer $500b$ over the entire uniform planar surface of the metal or other material layer 300 as illustrated in FIG. 5B.

[0047] Referring now to FIGS. 6A and 6B the removal of the nanodomains by etching leaving nanovoids in the poly mer is illustrated in greater detail. As illustrated in FIG. 6A, a mask is formed by removal of the nanodomains leaving holes 600 that extend through the polymer layer 400b. The nan odomains are removed by etching and nanovoids (holes) 600 are left in the polymer 400b. As illustrated in FIG. 6B, the nanovoids form a uniform hexagonal pattern of holes 600 over the entire polymer layer that extend through the polymer 400b.

[0048] Referring now to FIG. 7, the step of ion beam milling the metal or other material through the nano-voids of the mask producing nano-pores in the metal or other material is illustrated in greater detail. The holes 600 in the polymer layer 400b are used as a mask for ion beam milling the metal or other material layer 300.

[0049] As shown in FIG. 7, an ion beam milling machine 700 produces an ion beam 702 that ablates the metal or other material layer 300 exposed by the holes 600 in the mask. The ion beam milling of the metal or other material layer 300 through the holes 600 in the polymer layer 400b produces nano-pores in the metal or other material layer 300 creating the array. When the layer 300 is made of material other than metal, other physical etching techniques can be used to pro duce the nano-pores and create the array.

[0050] Referring now to FIGS. 8A and 8B, removal of the polymer layer mask leaving the nanoporous array is illus trated in greater detail. As illustrated in FIG. 8A, the polymer layer mask has been removed by dissolution leaving the nan oporous array. The ion beam milling of the metal or other material layer 300 through the holes in the polymer layer has produced nano-pores 800 in the metal or other material layer 300 creating the array. As illustrated in FIG. 8B, a hexagonal pattern of holes 800 is formed in the metal or other material layer 300. The array has use in batteries, ultracapacitors, other electrical devices, and any device that utilizes an array with nanopores.

[0051] Nanoporous Array

[0052] Referring now to FIG. 9, the inventor's nanolithog-raphy method for producing a nanoporous array is illustrated. The nanolithography method for producing a nanoporous array is designated generally by the reference numeral 900. The nanoporous array has use in batteries, ultracapacitors, other electrical devices, sensors, and any device that utilizes an array with nanopores. The inventor's array having nanopores possess a much higher Surface area suitable for better electron transfer providing improved performance of an elec trode in an electric double layer capacitor or a battery or a photovoltaic cell, and for sensing lower analyte concentra tions ins sensors in the like of Surface Enhanced Ramanor IR. [0053] As illustrated in FIG. 9, the first step is to provide a substrate. The substrate is designated by the reference numeral 901. A substrate of silicon or other material is pro vided. The substrate 901 has a flat surface. In one embodi ment the inventors used a 10 centimeter diameter silicon wafer as the substrate; however it is to be understood that other size silicon wafers and substrates of other materials can be used as the substrate. For example, substrates of silicon dioxide, aluminum oxide, sapphire, germanium, gallium arsenide, polyethylene terephthalate, polyethylene-naphthalate, polyimide, paper, foil can be used as the substrate. Substrates are chosen for the end use environment of the finished array. For example if a flexible array is to be produced the material for the substrate is chosen to be flexible.

[0054] The second step illustrated in FIG. 9 is to coat metal or other material on the surface of the substrate 901. A thin layer 902 of metal or other material is applied to the flat surface of the substrate 901 in a manner that provides a uniform planar surface on the metal or other material. This provides an exposed surface of the metal or other material for additional processing.

[0055] The surface of the layer metal or other material 902 is smooth. In determining the best roughness of surface 902 the inventors deposited Au on bare Si wafers with various thicknesses from 30 nm to 200 nm in order to obtain various surface roughness values. In a first sample, 30-nm-thick Au was deposited on a 30-nm-thick Pt layer. In additional samples, thicknesses of Au deposited directly on Si were 30, 50, 100, 150 and 200 nm, respectively. Au deposition rate for the first sample was faster than for the other samples. The roughness of the Authin film generally increases with the film thickness. The additional process still takes place even for a rather rough surface (Rrms>20 A), but it is actually the pore coverage that is strongly influenced by the metal film rough ness. The first sample was the smoothest sample (Rrms of 6.5 Å), the pore coverage was $91.9(\pm 1.1)\%$. Surprisingly, a slight variation in Rrms can give rise to considerable degradation in the pore coverage. With increased roughness, uniformity also decreases. Although the inventors had to deposit a thin film to control the surface roughness, they envisioned that it is possible to obtain large pore coverage even for thicker metal films by lowering the Surface roughness via optimization of deposition parameters. Strategies to improve the smoothness of as-deposited metal films encompass changing metal depo sition rate adjusting the temperature of a destination substrate coating a sticking agent layer prior to deposition, and per forming a template-striping method. The inventors also use metal other than gold for the nanoporous metal films.

[0056] In an attempt to assess the quality of the inventors nanoporous metal films, they defined a term, pore coverage, mentally and theoretically extrapolated for ideal conditions. This pore coverage measures 91.9% for the inventor's nan oporous metal films over a 10-cm-diameter wafer with a great uniformity value of 99%. The inventors characterize that the pore coverage becomes lower as the metal film gets rougher. In order to explain the relationship between pore coverage and roughness, the inventors introduced the effect of rough localities of the metal surface on BCP self-assembly by ana lyzing how they could impede the mobility of PS molecules thereby creating defect sites on the nanoporous PS and even tually on the nanoporous metal arrays. Finally, the inventors propose a method to estimate an expected pore coverage value for any given metal roughness by taking into account the areal density of the rough localities.

[0057] The third step illustrated in FIG. 9 is the step of coating a polymer layer on the layer 902 of the metal or other material and forming a mask for further processing. As shown, a polymer layer 903 is coated on the surface of the

layer 902 metal or other material. The polymer layer 903 will be used to create a mask for further processing.

0058. The polymer layer 903 is used to form a mask by combining a first polymer and a second polymer that form self-assembled nanodomains of the first polymer in the sec ond polymer. By selecting the composition of the first poly mer and the second polymer and by controlling the applica tion of the polymer layer the inventors have discovered that it is possible to pattern nanodomains of the first polymer in the second polymer. The application of the polymer layer results in the first polymer self-assembling into nanodomains of the first polymer in the second polymer. The self-assembly of the nanodomains results in the formation of a uniform hexagonal pattern of the first polymer nanodomains in the second poly mer over the entire uniform planar surface layer 902 of the metal or other material.

[0059] Removal of the nanodomains by etching leaves nanovoid holes 904 in the second polymer. The mask is formed by removal of the nanodomains leaving holes 904 that extend through the polymer layer 903. The nanodomains are removed by etching leaving the nanovoid holes 904 the poly mer 903. The nanovoid holes 904 form a uniform hexagonal pattern of holes 904 over the entire polymer layer 903 and the holes 904 extend through the polymer 903.

[0060] The fourth step illustrated in FIG. 9 is the step of ion beam milling. In the fourth step the holes 904 in the polymer layer 903 are used as a mask 906 for ion beam milling the metal or other material layer 902. The metal or other material is selectively removed by ion beam milling through the nano void holes 904 of the mask 906 producing nano-pore holes 904 in the metal or other material layer 902. An ion beam milling machine is used to ablate the metal or other material layer exposed by the holes 904 in the mask906. This produces nano-pores 907 in the metal or other material layer 902 cre ating the array.

0061] Nanoporous Array Battery

[0062] Referring now to FIG. 10, a nanolithography method for producing a nanoporous array battery is illus trated. The nanolithography method for producing a nanopo rous array battery is designated generally by the reference numeral 1000.

[0063] As illustrated in FIG. 10, substrates 1001 and 1007 are provided. The substrates 1001 and 1007 are made of an insulator material. Metal or other material is coated on the surfaces of substrates 1001 and 1007 to form the battery's anode and cathode.

[0064] The battery's anode is produced by applying a thin layer of anode material 1002 to the surface of the substrate 1001. A polymer layer is coated on the layerofanode material 1002 to form a mask for further processing. The polymer layer is used to form a mask by combining a first polymer and a second polymer that form self-assembled nanodomains of the first polymer in the second polymer. Removal of the nanodomains by etching leaves nanovoids in the second poly mer. The mask is formed by removal of the nanodomains leaving holes that extend through the polymer layer. The holes are used as a mask for ion beam milling the anode material layer 1002. This produces nano-pores 1003 in the anode material layer 1002. The mask material is removed leaving the battery's anode 1002 that includes the nano-pores 1003. The anode 1002 with nano-pores 1003 possess a much higher surface area and provides better electron transfer and improved performance of the 1000 battery.

 $[0065]$ The battery's cathode is produced by applying a thin layer of cathode material 1005 to the surface of the substrate 1007. A polymer layer is coated on the layer of cathode material 1005 to form a mask for further processing. The polymer layer is used to form a mask by combining a first polymer and a second polymer that form self-assembled nan odomains of the first polymer in the second polymer. Removal of the nanodomains by etching leaves nanovoids in the second polymer. The mask is formed by removal of the nanodomains leaving holes that extend through the polymer layer. The holes are used as a mask for ion beam milling the cathode material layer 1005. This produces nano-pores 1006 in the cathode material layer 1005. The mask material is removed leaving the battery's cathode 1005 that includes the nano-pores 1006. The cathode 1005 with nano-pores 1006 possess a much higher surface area and provides better electron transfer and improved performance of the 1000 battery. [0066] An electrolyte 1004 is positioned between the battery's anode 1002 and battery's cathode 1005. An electrical lead 1008 is attached to the battery's anode 1002 by connec tion 1008. An electrical lead 1011 is attached to the battery's cathode 1007 by connection 1012. The electrical lead 1009 and electrical lead 1011 are connected across a load 1010 that is powered by the inventor's battery 1000. In other embodi ments of the nanoporous battery 1000, the anode 1002 or the cathode 1005 are made of a standard anode or cathode mate rial.

[0067] Photovoltaic Cell

[0068] Referring again to FIG. 10, instead of a battery, a photovoltaic cell can be produced by using an active photo voltaic material 1004 instead of the electrolyte material. The substrate 1001 is made of a material that is transparent to light and the electrode 1002 includes nano-pores 1003 making the electrode 1002 transparent to light. This further enhances the light absorption by the active photovoltaic material 1004 by means of the plasmonic enhancement effect, which enhances the electric field of the light within at the edges and surfaces of the pores. In one embodiment the substrate 1001 and the thin layer of material 1002 applied to the surface of the substrate 1001 are made of a material that is transparent to light. In one embodiment, the photovoltaic cell's electrode 1002 is made of a transparent metal oxide to allow light to be absorbed by the active photovoltaic material 1004.

[0069] The photovoltaic cell is made by a nanolithography method that includes providing substrates 1001 and 1007. One or both of the Substrates 1001 and 1007 are made of made of a material that is transparent to light. Metal or other mate rial is coated on the surfaces of substrates 1001 and 1007 to form the photovoltaic cell's electrodes.

[0070] An active photovoltaic material 1004 is positioned between the photovoltaic cell's electrode 1002 and the pho tovoltaic cell's electrode 1005. An electrical lead 1008 is attached to the photovoltaic cell's electrode 1002 by connection 1008. An electrical lead 1011 is attached to the photovoltaic cell's electrode 1007 by connection 1012. The electrical lead 1008 and electrical lead 1011 are connected across a load 1010 that is powered by the active photovoltaic mate rial 1004.

[0071] Nanoporous Filter

[0072] Referring now to FIGS. 11A and 11B, embodiments of nanolithography methods for producing nanoporous filters are illustrated. The nanolithography methods are designated generally by the reference numeral 1100. In one method a nanoporous array is formed on a porous substrate producing a nanoporous filter. In another method, the nanoporous array is removed from the substrate providing a nanoporous filter. [0073] One nanolithography method of producing a nanoporous filter is illustrated in FIG. 11A. A substrate made of a porous material 1102 is provided. A thin layer of metal or other material is applied to the surface of the substrate. The thin layer 1104 will serve as the matrix of the filter. A mask is created on the surface of the thin layer 1104 by combining a first polymer and a second polymer to form a polymer layer (not shown) of the first and second polymer. The first polymer self-assembles into nanodomains of the first polymer in the second polymer. The self-assembly of the nanodomains results in the formation of a uniform hexagonal pattern of the first polymer nanodomains in the second polymer over the surface on the thin layer 1104. The nanodomains are removed by etching to form nano-Voids that extend through the poly mer layer. Nanopores are created in the thin layer 1104 by ion beam milling the thin layer material through the nano-Voids to produce nano-pores 1106 that extend through the thin layer 1104 creating the array 1100 having nanopores 1106. The nanopores 1106 in the thin layer 1104 matrix and the flexible material substrate 1102 provide a nanoporous filter.

[0074] Referring to FIG. 11B, another nanolithography method of producing a nanoporous filter is illustrated. The steps of providing a substrate 1102 and coating a thin layer 1104 of metal or other on the surface of the substrate are performed. A mask is created on the thin layer 1104 by combining a first polymer and a second polymer to form a polymer layer (not shown) of the first and second polymer that self-assemble into nanodomains of the first polymer in the second polymer forming a uniform hexagonal pattern of the first polymer nanodomains in the second polymer over the surface on the thin layer 1104. The nanodomains are removed by etching to form nano-Voids that extend through the poly mer layer. Nanopores are created in the thin layer 1104 by ion beam milling the thin layer material through the nano-Voids to produce nano-pores 1106 that extend through the thin layer 1104. The thin layer 1104 matrix with the nanopores 1106 is removed from the substrate 1102 providing a filter.

[0075] Although the description above contains many details and specifics, these should not be construed as limiting the scope of the application but as merely providing illustrations of some of the presently preferred embodiments of the apparatus, systems, and methods. Other implementations, enhancements and variations can be made based on what is described and illustrated in this patent document. The fea tures of the embodiments described herein may be combined in all possible combinations of methods, apparatus, modules, systems, and computer program products. Certain features that are described in this patent document in the context of separate embodiments can also be implemented in combina tion in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as Such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination. Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be per

formed, to achieve desirable results. Moreover, the separation of various system components in the embodiments described above should not be understood as requiring such separation in all embodiments.

 $[0076]$ Therefore, it will be appreciated that the scope of the present application fully encompasses other embodiments which may become obvious to those skilled in the art. In the claims, reference to an element in the singular is not intended to mean "one and only one' unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device to address each and every problem sought to be solved by the present apparatus, systems, and methods, for it to be encompassed by the present claims. Furthermore, no element or component in the present disclo sure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the claims. No claim element herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the ele ment is expressly recited using the phrase "means for."

[0077] While the apparatus, systems, and methods may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. How ever, it should be understood that the application is not intended to be limited to the particular forms disclosed. Rather, the application is to cover all modifications, equiva lents, and alternatives falling within the spirit and scope of the application as defined by the following appended claims.

1. A nanolithography method for creating an array, com prising the steps of:

providing a substrate having surface;

- coating a layer of material on said surface of said substrate providing a material surface;
- forming a mask on said material surface by combining a first polymer and a second polymer to form self-as sembled nanodomains of said first polymer in said sec ond polymer and removing said nanodomains to form nano-voids in said mask; and
- ion beam milling said material through said nano-Voids in said mask producing nano-pores in said material creat ing the array.

2. The nanolithography method for creating an array of claim 1 wherein said step of coating a layer of material on said surface of said substrate providing a material surface comprises controlling the coating of a layer of material on said surface of said substrate to produce said material surface that has a roughness in the range of Rrms 6.0 A to Rrms 20 A.

3. The nanolithography method for creating an array of claim 1 wherein said step of coating a layer of material on said surface of said substrate providing a material surface comprises controlling the coating of a layer of material on said surface of said substrate to produce said material surface that has a roughness in the range of Rrms 6.0 A to Rrms 7.0 A.

4. The nanolithography method for creating an array of claim 1 wherein said step of coating a layer of material on said surface of said substrate providing a material surface comprises controlling the coating of a layer of material on said surface of said substrate to produce said material surface that has a roughness of Rrms 6.5 A.

5. The nanolithography method for creating an array of claim 1 wherein said step of coating a layer of material on said surface of said substrate providing a material surface comprises coating a layer of metal on said surface of said Substrate providing a metal surface.

6. The nanolithography method for creating an array of claim 5 wherein said metal comprises gold, silver, or alumi num.

7. The nanolithography method for creating an array of claim 1 wherein said step of coating a layer of material on said surface of said substrate providing a material surface comprises coating a layer of flexible metal on said surface of said substrate providing a flexible metal surface.

8. The nanolithography method for creating an array of claim 1 wherein said step of forming a mask on said material surface comprises combining a first polymer and a second polymer to form self-assembled cylindrical nanodomains of said first polymer in said second polymer and removing said cylindrical nanodomains to form cylindrical nano-voids in said mask.

9. The nanolithography method for creating an array of claim 1 wherein said step of forming a mask on said material surface comprises combining a first polymer and a second polymer to form self-assembled cylindrical nanodomains of said first polymer in said second polymer and removing said cylindrical nanodomains to form cylindrical nano-voids in said mask and wherein said step of ion beam milling said material through said nano-voids in said mask comprises ion beam milling said material through said cylindrical nano Voids in said mask.

10. The nanolithography method for creating an array of claim 1 wherein said step of forming a mask on said material surface comprises combining a first polymer and a second polymer to form self-assembled spherical nanodomains of said first polymer in said second polymer and removing said spherical nanodomains to form nano-voids in said mask.

11. The nanolithography method for creating an array of claim 1 wherein said step of combining a first polymer and a second polymer to form self-assembled nanodomains of said first polymer in said second polymer and removing said man odomains to form nano-Voids in said mask comprises com bining a first polymer and a second polymer to form self assembled nanodomains of said first polymer in said second polymer in a hexagonal pattern of said nanodomains of said first polymer in said second polymer and removing said man odomains to form a hexagonal pattern of said nano-voids in said mask.

12. The nanolithography method for creating an array of claim 11 wherein said step of ion beam milling said material through said nano-Voids in said mask comprises ion beam milling said material through said hexagonal pattern of said nano-voids in said mask producing a hexagonal pattern of said nano-pores in said material creating the array.

13. The nanolithography method for creating an array of claim 1 wherein said step of providing a substrate having surface comprises providing a substrate of silicon having a silicon surface.

14. The nanolithography method for creating an array of claim 1 wherein said step of providing a substrate having surface comprises providing a substrate of a porous material having a porous material surface.

15. The nanolithography method for creating an array of claim 1 wherein said step of providing a substrate having surface comprises providing a substrate of a flexible material having a flexible material surface.

16. A nanolithography method for producing a battery, comprising the steps of

- providing an anode substrate having an anode substrate surface,
- coating a layer of anode material on said anode substrate surface providing an anode material surface,
- forming a mask on said anode material surface by combining a first polymer and a second polymer to form self assembled nanodomains of said first polymer in said second polymer and removing said nanodomains to form nano-voids in said mask,
- ion beam milling said anode material through said nano Voids in said mask producing nano-pores in said anode material creating an anode array of said anode substrate and said anode material with nano-pores,
- providing a cathode substrate having a cathode substrate surface,
- coating a layer of cathode material on said cathode substrate surface providing a cathode material surface,
- forming a mask on said cathode material surface by combining a first polymer and a second polymer to form self-assembled nanodomains of said first polymer in said second polymer and removing said nanodomains to form nano-voids in said mask,
- ion beam milling said cathode material through said nano Voids in said mask producing nano-pores in said cathode material creating a cathode array of said cathode substrate and said cathode material with nano-pores,
- providing an electrolyte between said anode array and said cathode array,
- and connecting a circuit between said anode array and said cathode array producing the battery.

17. The nanolithography method for producing a battery of claim 16 wherein the step of providing an anode substrate comprises providing an anode Substrate made of an insulator material and wherein the step of providing a cathode substrate comprises providing an cathode substrate made of an insula tor material.

18. A nanolithography method for producing a filter, com prising the steps of:

providing a substrate having a substrate surface,

- coating a layer of metal or other material on said substrate surface providing a metal or other material surface,
forming a mask on said metal or other material surface by
- combining a first polymer and a second polymer to form self-assembled nanodomains of said first polymer in said second polymer and removing said nanodomains to form nano-voids in said mask, and
- ion beam milling said metal or other material through said nano-voids in said mask producing nano-pores in said metal or other material creating an array of said porous substrate and said metal or other material with nanopores to produce said filter.

19. The nanolithography method for producing a filter of claim 18 wherein said step of wherein said step of coating a layer of material on said surface of said substrate providing a metal or other material Surface comprises controlling the coating of a layer of metal or other material on said surface of said substrate to produce said metal or other material surface that has a roughness in the range of Rrms 6.0 A to Rrms 20 A.

20. The nanolithography method for producing a filter of claim 18 wherein said step of coating a layer of metal or other

material on said surface of said Substrate providing a metal or other material Surface comprises controlling the coating of a layer of metal or other material on said surface of said sub strate to produce said metal or other material surface that has a roughness in the range of Rrms 6.0 A to Rrms 7.0 A.

21. The nanolithography method for producing a filter of claim 18 wherein said step of coating a layer of metal or other material on said surface of said Substrate providing a metal or other material Surface comprises controlling the coating of a layer of metal or other material on said surface of said sub strate to produce said metal or other material surface that has a roughness of Rrms 6.5 A.

22. The nanolithography method for producing a filter of claim 18 wherein said step of forming a mask on said metal or other material surface comprises combining a first polymer and a second polymer to form self-assembled cylindrical nanodomains of said first polymer in said second polymer and
removing said cylindrical nanodomains to form cylindrical nano-voids in said mask.

23. The nanolithography method for producing a filter of claim 18 wherein said step of forming a mask on said metal or other material surface comprises combining a first polymer and a second polymer to form self-assembled cylindrical nanodomains of said first polymer in said second polymer and removing said cylindrical nanodomains to form cylindrical nano-voids in said mask and wherein said step of ion beam milling said metal or other material through said nano-voids in said mask comprises ion beam milling said metal or other material through said cylindrical nano-Voids in said mask.

24. The nanolithography method for producing a filter of claim 18 wherein said step of combining a first polymer and a second polymer to form self-assembled nanodomains of said first polymer in said second polymer and removing said nanodomains to form nano-voids in said mask comprises combining a first polymer and a second polymer to form self-assembled nanodomains of said first polymer in said second polymer in a hexagonal pattern of said nanodomains of said first polymer in said second polymer and removing said nanodomains to form a hexagonal pattern of said nano Voids in said mask.

25. The nanolithography method for producing a filter of claim 18 wherein said step of ion beam milling said metal or other material through said nano-voids in said mask com said hexagonal pattern of said nano-voids in said mask producing a hexagonal pattern of said nano-pores in said metal or other material creating the array.

other material creating the array. k k k k k